

# H256A-S

**Wi-Fi Dual-band 1X1 802.11a/b/g/n**

**Module Datasheet**



## H256A-S Module Datasheet

**Office:** 6 Floor, Building U6, Junxiang U8 Park,  
Hangcheng Avenue, Bao'an District,  
Shenzhen City, CHINA

**Factory:** No.8, Litong Road, Liuyang Economic & Technical  
Development Zone, Changsha, Hunan, CHINA

**TEL:** +86-755-2955-8186

**Website:** [www.fn-link.com](http://www.fn-link.com)

Customer Approval : \_\_\_\_\_ Company  
\_\_\_\_\_  
Title  
\_\_\_\_\_  
Signature  
\_\_\_\_\_  
Date  
\_\_\_\_\_  
Fn-Link

## Revision History

Version	Date	Revision Content	Draft	Approved
1.0	2020/10/09	New version	Lxy	Szs
1.1	2021/06/24	Update module photo	Lxy	QJP

# CONTENTS

<b>1 Overview.....</b>	<b>1</b>
1.1 Introduction.....	1
1.2 Features.....	1
1.3 General Specification.....	1
1.4 Recommended Operating Rating.....	2
1.5 Current informations.....	2
※1.6 EEPROM Information.....	2
<b>2 General Specification.....</b>	<b>2</b>
2.1 Wi-Fi RF Specifications.....	2
<b>3 Pin Assignments.....</b>	<b>5</b>
3.1 Pin Outline.....	5
3.2 Pin Definition.....	6
<b>4 Dimensions.....</b>	<b>7</b>
4.1 Module Picture.....	7
4.2 Marking Description.....	7
4.3 Module Physical Dimensions.....	7
4.4 Layout Reference.....	8
<b>6 Host Interface Timing Diagram.....</b>	<b>9</b>
6.1 SDIO Pin Description.....	9
6.2 SDIO Default Mode Timing Diagram.....	10
6.3 SDIO Power-on sequence.....	10
<b>7 Reference Design.....</b>	<b>12</b>
<b>8 Ordering Information.....</b>	<b>13</b>
<b>9 The Key Material List.....</b>	<b>13</b>
<b>10 Environmental Requirements.....</b>	<b>13</b>
10.1 Recommended Reflow Profile.....	13
10.2 Patch Wi-Fi modules installed before the notice.....	14
<b>11 Package.....</b>	<b>15</b>
11.1 Reel.....	15
11.2 Packaging Detail.....	16

# 1 Overview

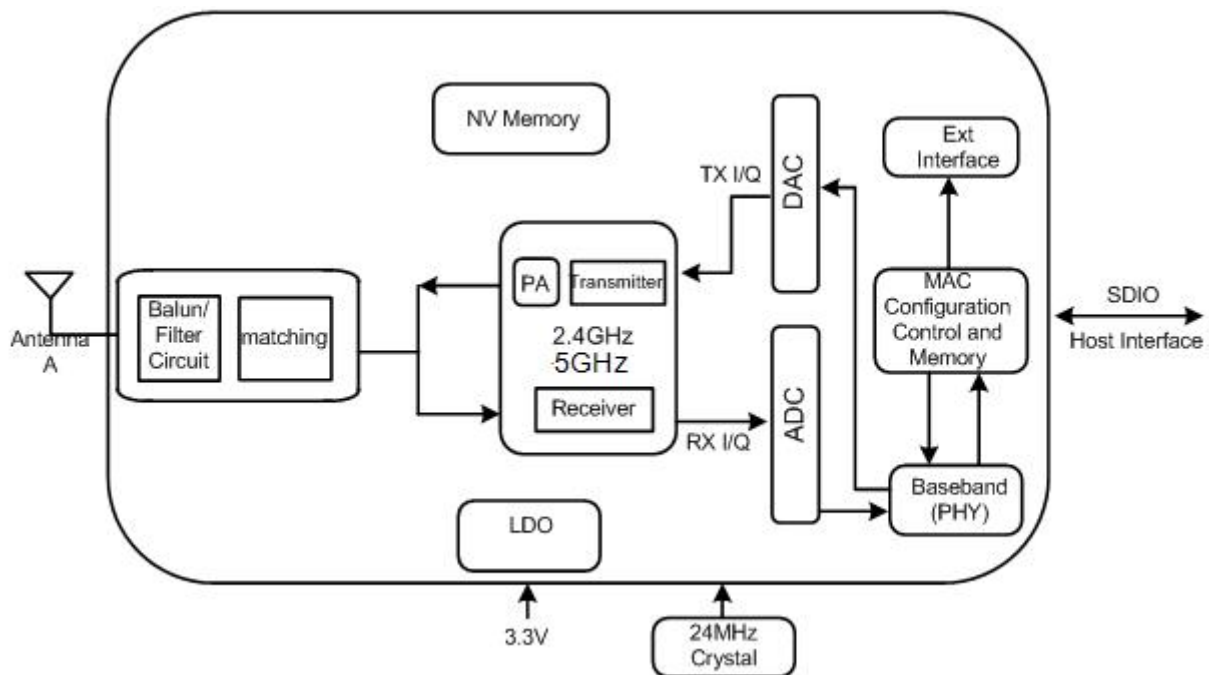
## 1.1 Introduction

H256A-S is a highly integrated and excellent performance Wireless LAN (WLAN) SDIO network interface device. Based on iCOMM chipset SV6256P. support 802.11a/b/g/n standard.

## 1.2 Features

- Operate at ISM frequency bands (2.4GHz+5GHz)
- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11a/b/g/n compatible WLAN
- Wi-Fi 1 T 1 R allow data rates supporting up to 150 Mbps PHY rates

### Block Diagram:



## 1.3 General Specification

Model Name	H256A-S
Product Description	Support Wi-Fi functionalities
Dimension	L x W x T: 12 x 12 x 1.6 (typical) mm
Wi-Fi Interface	Support SDIO
Operating temperature	-10°C to 70°C

Storage temperature	-40°C to +85°C
---------------------	----------------

## 1.4 Recommended Operating Rating

	Min.	Typ.	Max.	Unit
Operating Temperature	-10	25	70	deg.C
VBAT	3.0	3.3	3.6	V
VDDIO	1.7	1.8 or 3.3	3.6	V

## 1.5 Current informations

Vcc=3.3V, Ta=25° C, unit: mA		
current	TX mode	RX mode
802.11b 11Mbps	279.2	114
802.11g 54Mbps	241.8	114.3
802.11n HT20 MCS7	241.3	113.6
802.11n HT40 MCS7	245.3	125.3
802.11g 54Mbps	281.4	142.2
802.11n HT20 MCS7	280.9	142.3
802.11n HT40 MCS7	285.4	153

## ※1.6 EEPROM Information

WI-FI

Vendor ID	-
Product ID	-

## 2 General Specification

### 2.1 Wi-Fi 2.4G RF Specifications

Feature	Description
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)
Number of Channels	2.4GHz: Ch1 ~ Ch14

Spectrum Mask	Min. b/g/n	Typ. b/g/n	Max. b/g/n	Unit b/g/n
1st side lobes(to fc ± 11MHZ)	-	-43/-30/-40	-	dBr
2st side lobes(to fc ± 22MHZ)	-	-52/-33/-58	-	dBr
Freq. Tolerance	-20/-20/-20	-	20/20/20	ppm
Test Items	Typical Value			EVM
Output Power	802.11b /11Mbps : 17dBm ± 2 dB			EVM ≤ -9dB
	802.11g /54Mbps : 13dBm ± 2 dB			EVM ≤ -26dB
	802.11n /MCS7 : 13dBm ± 2 dB			EVM ≤ -28dB
Test Items	TYP Test Value			Standard Value
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps	PER @ -92 dBm		≤-83
	- 2Mbps	PER @ -90 dBm		≤-80
	- 5.5Mbps	PER @ -87 dBm		≤-79
	- 11Mbps	PER @ -85 dBm		≤-76
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps	PER @ -89 dBm		≤-85
	- 9Mbps	PER @ -88 dBm		≤-84
	- 12Mbps	PER @ -87 dBm		≤-82
	- 18Mbps	PER @ -84 dBm		≤-80
	- 24Mbps	PER @ -81 dBm		≤-77
	- 36Mbps	PER @ -78 dBm		≤-73
	- 48Mbps	PER @ -73 dBm		≤-69
	- 54Mbps	PER @ -71 dBm		≤-68
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -87 dBm		≤-85
	- MCS=1	PER @ -84 dBm		≤-82
	- MCS=2	PER @ -82 dBm		≤-80
	- MCS=3	PER @ -78 dBm		≤-77
	- MCS=4	PER @ -75 dBm		≤-73
	- MCS=5	PER @ -70 dBm		≤-69
	- MCS=6	PER @ -69 dBm		≤-68
	- MCS=7	PER @ -68 dBm		≤-67
SISO Receive Sensitivity (11n ,40MHz) @10% PER	- MCS=0,	PER @ -86 dBm		≤-82
	- MCS=1,	PER @ -83 dBm		≤-79
	- MCS=2,	PER @ -81 dBm		≤-77
	- MCS=3,	PER @ -78 dBm		≤-74
	- MCS=4,	PER @ -74 dBm		≤-70
	- MCS=5,	PER @ -69 dBm		≤-66
	- MCS=6,	PER @ -68 dBm		≤-65

	- MCS=7, PER @ -66 dBm	≤-64
Maximum Input Level	802.11b : -10 dBm	
	802.11g/n : -20 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

## 2.2 5GHz RF Specification

Feature	Description			
WLAN Standard	IEEE 802.11 a/n Wi-Fi compliant			
Frequency Range	5150MHz ~ 5850 GHz (5 GHz Band)			
Spectrum Mask	Min. b/g/n	Typ. b/g/n	Max. b/g/n	Unit b/g/n
1st side lobes(to fc ± 11MHZ)	-	-43/-30/-40	-	dBr
2st side lobes(to fc ± 22MHZ)	-	-52/-33/-58	-	dBr
Freq. Tolerance	-20/-20/-20	-	20/20/20	ppm
Test Items	Typical Value			EVM
Output Power	802.11a /54Mbps : 12dBm ± 2 dB			EVM ≤ -26dB
	802.11n /MCS7 : 12dBm ± 2 dB			EVM ≤ -28dB
Test Items	TYP Test Value			Standard Value
SISO Receive Sensitivity (11a,20MHz) @10% PER	- 6Mbps	PER @ -89 dBm	≤-85	
	- 9Mbps	PER @ -88 dBm	≤-84	
	- 12Mbps	PER @ -87 dBm	≤-82	
	- 18Mbps	PER @ -84 dBm	≤-80	
	- 24Mbps	PER @ -81 dBm	≤-77	
	- 36Mbps	PER @ -78 dBm	≤-73	
	- 48Mbps	PER @ -73 dBm	≤-69	
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -87 dBm	≤-85	
	- MCS=1	PER @ -84 dBm	≤-82	
	- MCS=2	PER @ -82 dBm	≤-80	
	- MCS=3	PER @ -78 dBm	≤-77	
	- MCS=4	PER @ -75 dBm	≤-73	
	- MCS=5	PER @ -70 dBm	≤-69	
	- MCS=6	PER @ -69 dBm	≤-68	
SISO Receive Sensitivity (11n ,40MHz) @10% PER	- MCS=0,	PER @ -86 dBm	≤-82	
	- MCS=1,	PER @ -83 dBm	≤-79	

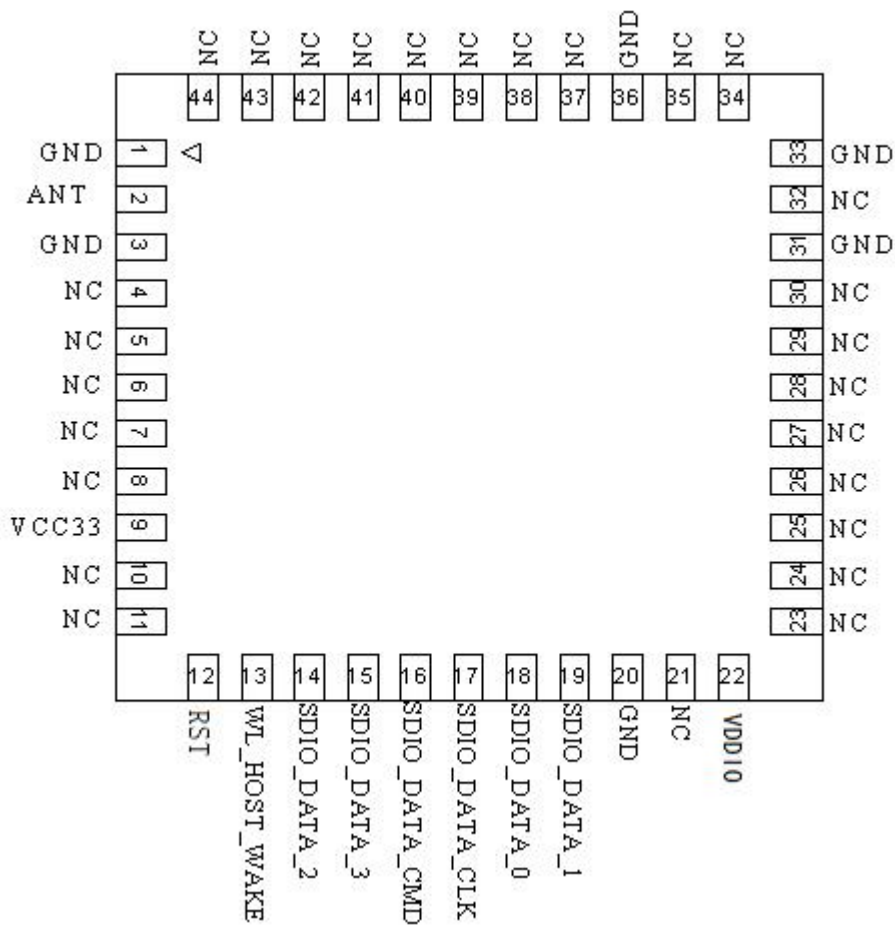


	- MCS=2, PER @ -81 dBm	≤-77
	- MCS=3, PER @ -78 dBm	≤-74
	- MCS=4, PER @ -74 dBm	≤-70
	- MCS=5, PER @ -69 dBm	≤-66
	- MCS=6, PER @ -68 dBm	≤-65
	- MCS=7, PER @ -66 dBm	≤-64
Maximum Input Level	802.11a/n : -20 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

### 3 Pin Assignments

#### 3.1 Pin Outline

<TOP>



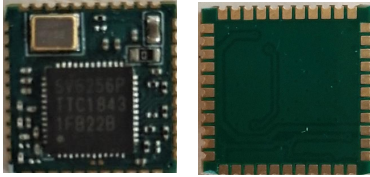
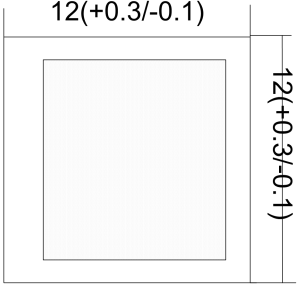

### 3.2 Pin Definition

Pin #	Name	Description
1	GND	GND
2	ANT	RF OUTPUT
3	GND	GND
4~8	NC	NC
9	VCC33	3.3V IN
10~11	NC	NC
12	RST	Reset, active low
13	WL_HOST_WAKE	WLAN WAKE HOST
14	SDIO_DATA_2	SDIO_D2
15	SDIO_DATA_3	SDIO_D3
16	SDIO_DATA_CMD	SDIO_CMD
17	SDIO_DATA_CLK	SDIO_CLK
18	SDIO_DATA_D0	SDIO_D0
19	SDIO_DATA_D1	SDIO_D1
20	GND	GND
21	NC	NC
22	VDIO	1.8 or 3.3V
23~30	NC	NC
31	GND	GND
32	NC	NC
33	GND	GND
34~35	NC	NC
36	GND	GND
37~44	NC	NC

P:POWER I:INPUT O:OUTPUT

## 4 Dimensions

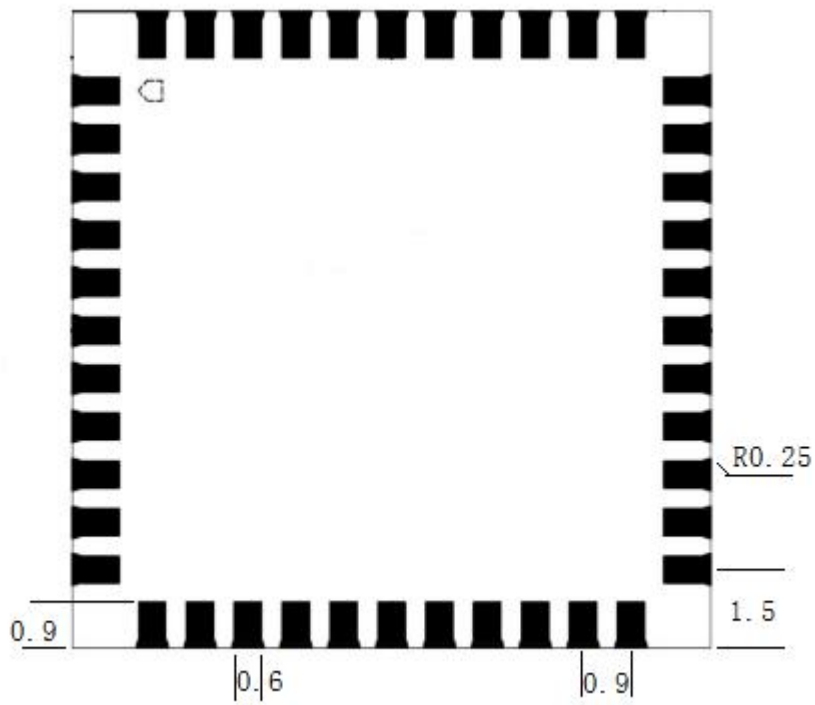
### 4.1 Module Picture

<p>L x W : 12 x 12 (+0.3/-0.1) mm</p> 	
<p>H: 1.6 (±0.2) mm</p>	
<p><b>Weight</b></p>	<p>0.38g</p>

### 4.2 Marking Description

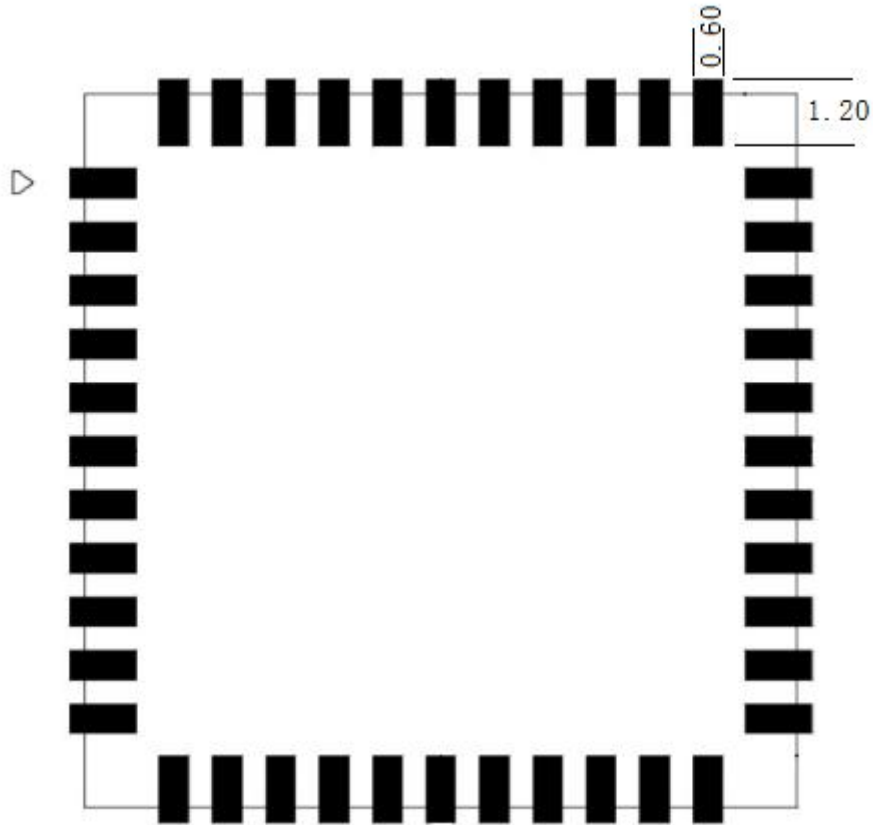
NA

### 4.3 Module Physical Dimensions



## 4.4 Layout Reference

(unit: mm )



## 6 Host Interface Timing Diagram

### 6.1 SDIO Pin Description

The module supports SDIO version 2.0 for all 1.8V 4-bit UHSI speeds: SDR12(25 Mbps), and SDR25(50Mbps) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz).

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock

CMD	Command Line
-----	--------------

## 6.2 SDIO Default Mode Timing Diagram

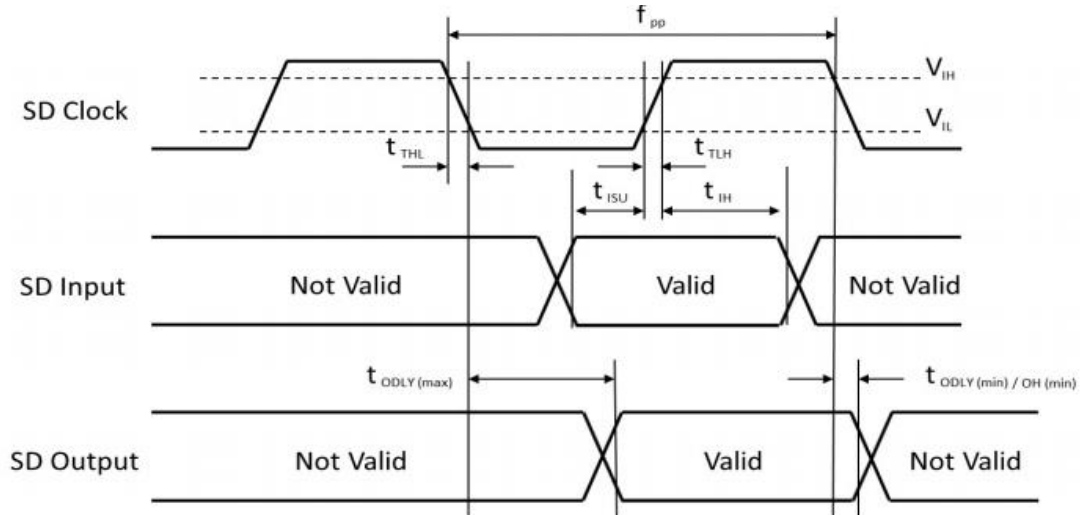


Figure 7 : SDIO TIMING WAVEFORM

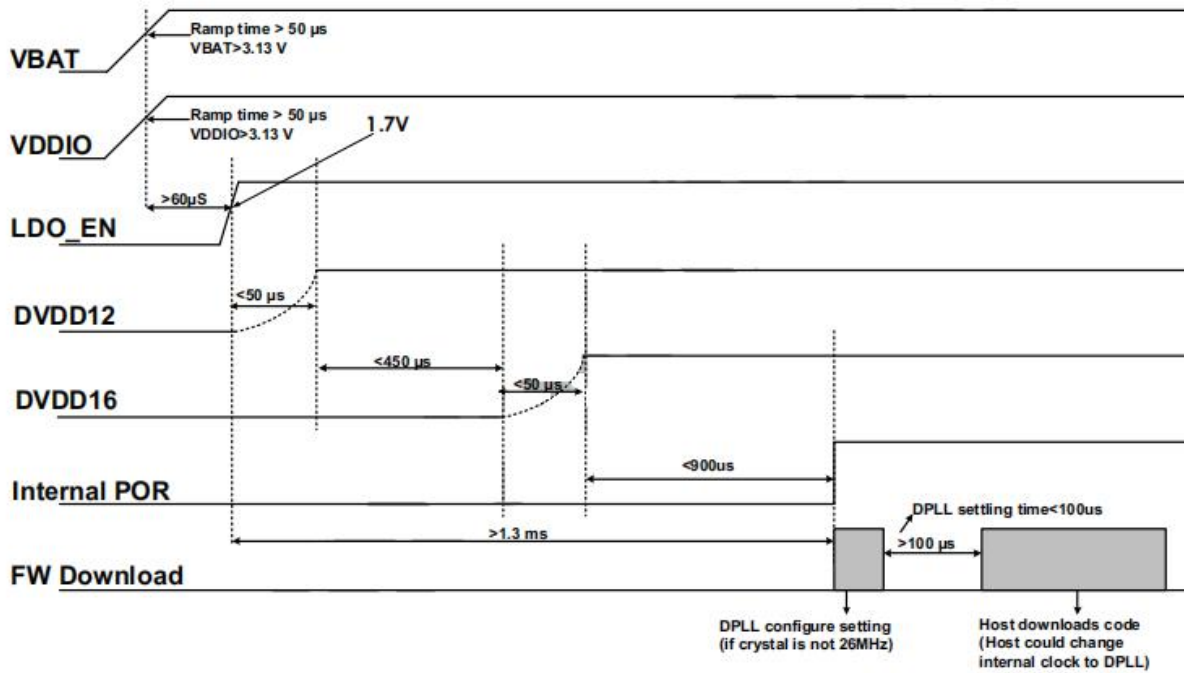
Table 4 : SV6152P SDIO version 2.0 Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
<b>Clock CLK (All values are referred to min(V<sub>IH</sub>) and max(V<sub>IL</sub>).</b>					
f <sub>pp</sub>	Clock frequency Data Transfer Mode	0		50	MHz
t <sub>TLH</sub>	Clock rise time			3	ns
t <sub>THL</sub>	Clock fall time			3	ns
<b>Inputs CMD, DAT (reference to CLK)</b>					
t <sub>ISU</sub>	Input set-up time	6			ns
t <sub>IH</sub>	Input hold time	2			ns
<b>Outputs CMD, DAT (reference to CLK)</b>					
t <sub>ODLY</sub>	Output Delay time during Data Transfer Mode			14	ns
t <sub>OH</sub>	Output Hold time	2.5			Ns

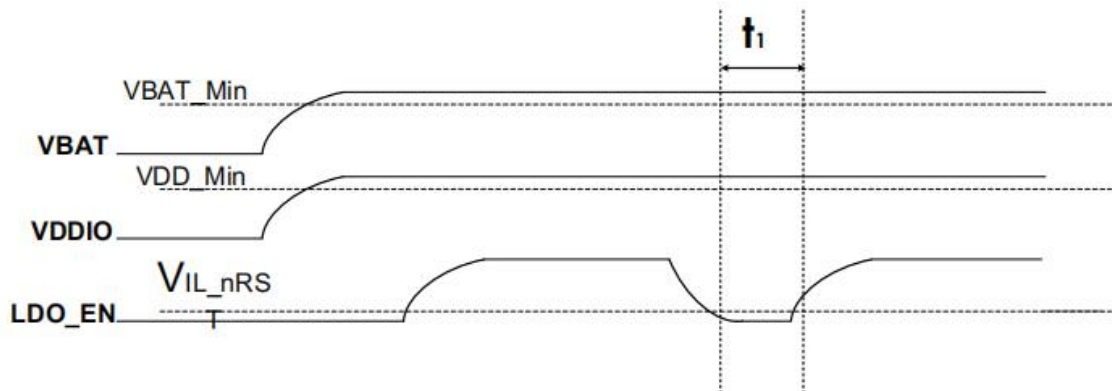
## 6.3 SDIO Power-on sequence

Figure 4 shows the power-on sequence of the SV615XP from power-up to firmware download, including the initial device power-on reset evoked by LDO\_EN signal. The LDO\_EN input level must be kept the same as VDDIO voltage level. After initial power-on, the LDO\_EN signal can be held low to turn off the SV615XP or pulsed low to induce a subsequent reset. After LDO\_EN is assert and host starts the power-on sequence of the SV615XP. From that point, the typical SV615XP power-on sequence is shown below:

1. Within 1.3 millisecond, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.



**Figure 4 : Power-on sequence**



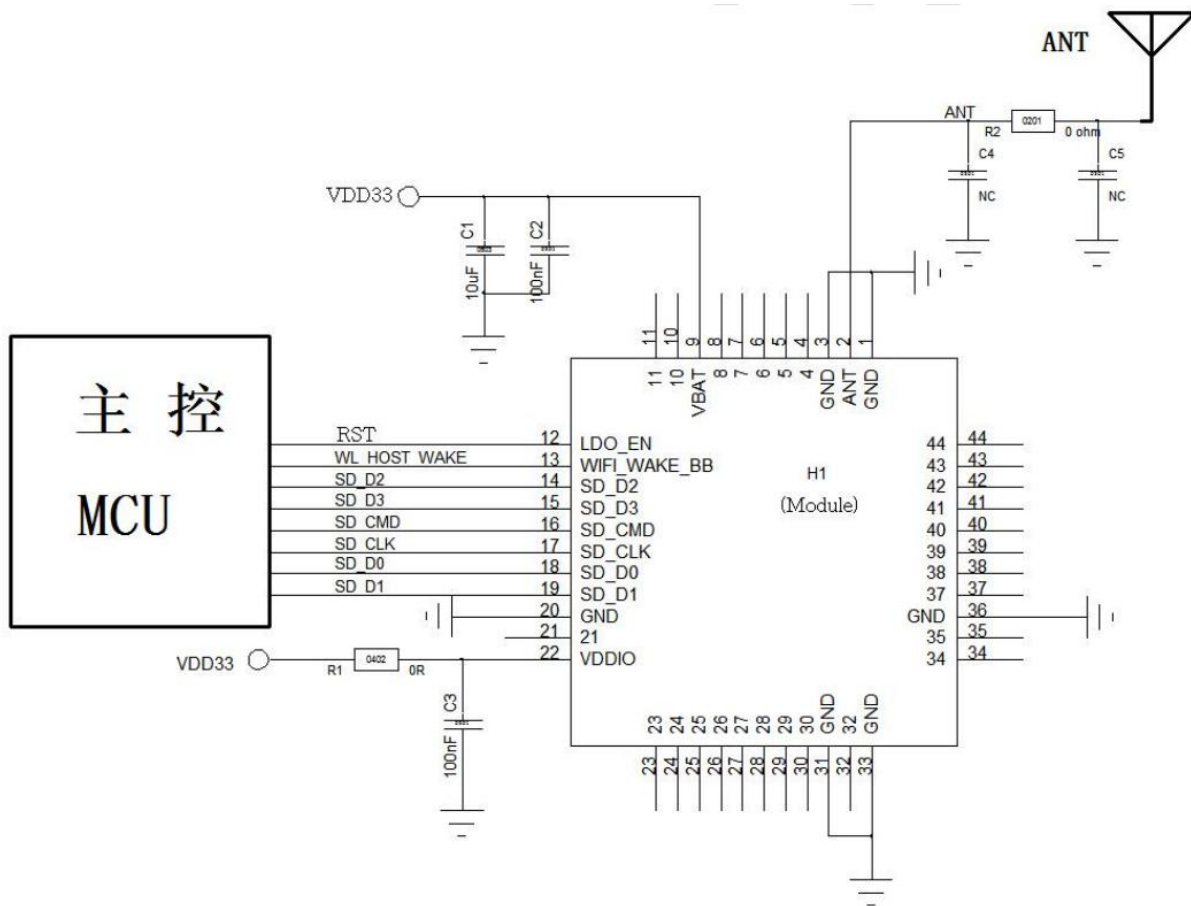
**Figure 5 : Reset Timing**

**Table 2 : Reset Timing Parameters**

Parameters	Description	Min.	Unit
t1	Duration of LDO_EN signal level $< V_{IL\_nRST}$ to reset the chip	30	us

The SV615XP LDO\_EN pin can be used to completely reset the entire chip. After this signal has been de-asserted, the SV615XP is in off mode waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules are held in reset. Once the host has initiated communication, the SV615XP turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

## 7 Reference Design



Note:

1. RF trace as short as possible .
2. Keep antenna away from metal componet.



## 8 Ordering Information

Part No.	Description
FGH256ASXX-00	SV6256P, a/b/g/n, WiFi 2.4G, 1T1R, SDIO, 单天线, 无屏蔽盖

## 9 The Key Material List

Crystal	3225 24MHZ CL=12pF, 10ppm	ECEC, TKD, Hosonic, JWT
PCB	H152A-S-V1.0 green, 4L, FR4, Tg150, AU, 30pcs, 12X12X0.6mm	XY-PCB, KX-PCB, SL-PCB, Sunlord
Chipset	SV6256P, 802.11a/b/g/n, SDIO Interface, QFN48L, 6x6xmm	iComm-semi

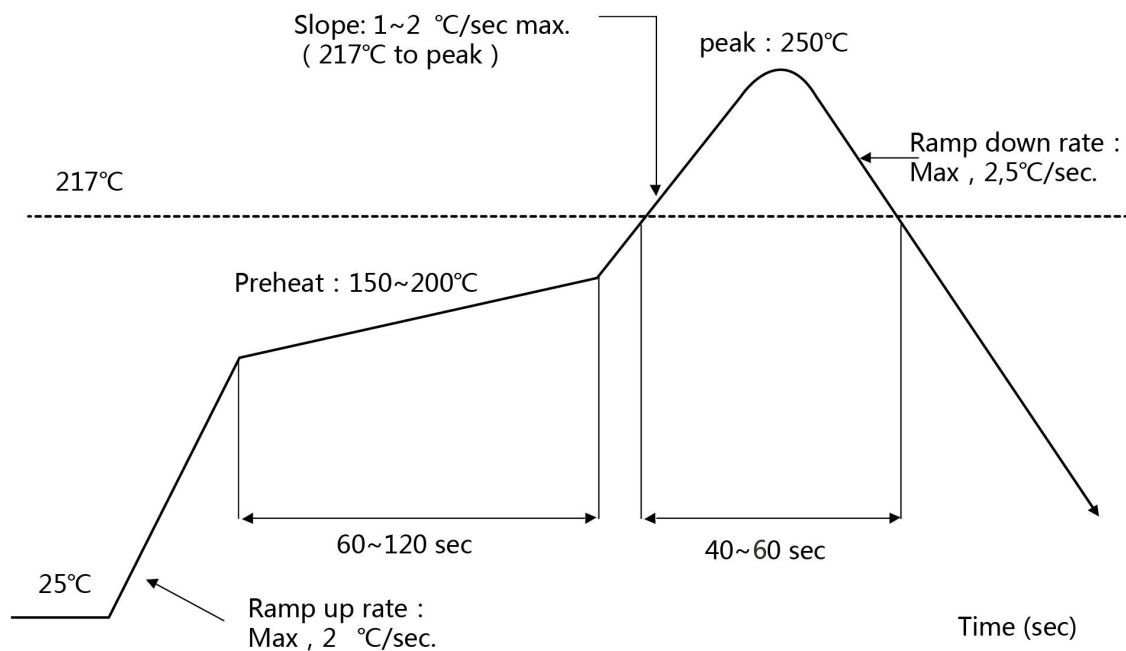
## 10 Environmental Requirements

### 10.1 Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



## 10.2 Moisture Sensitivity

The module is a Moisture Sensitive Level 3 device, in accordance with standard IPC/JEDEC J-STD-020, take care of all the requirements for this kind of components.

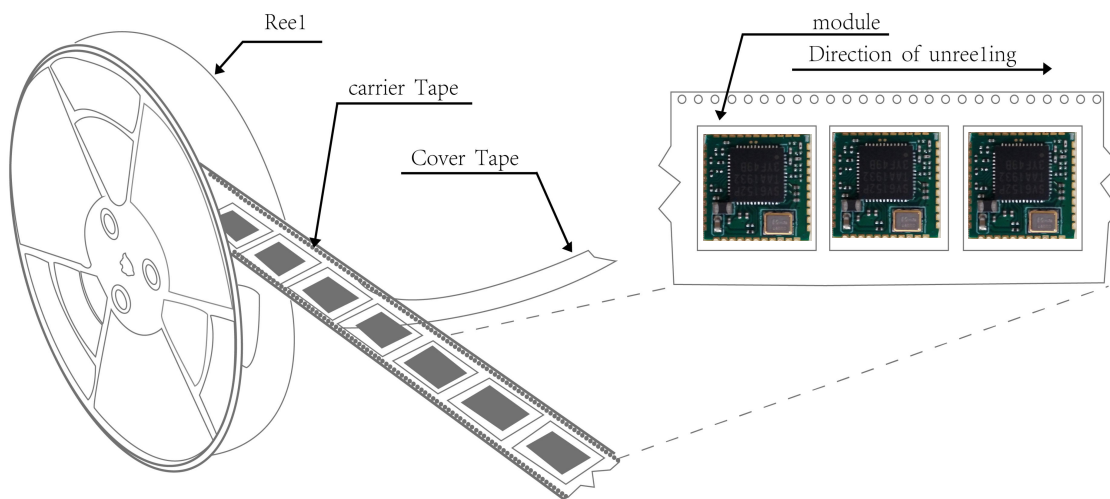
Moreover, please pay attention to following conditions:

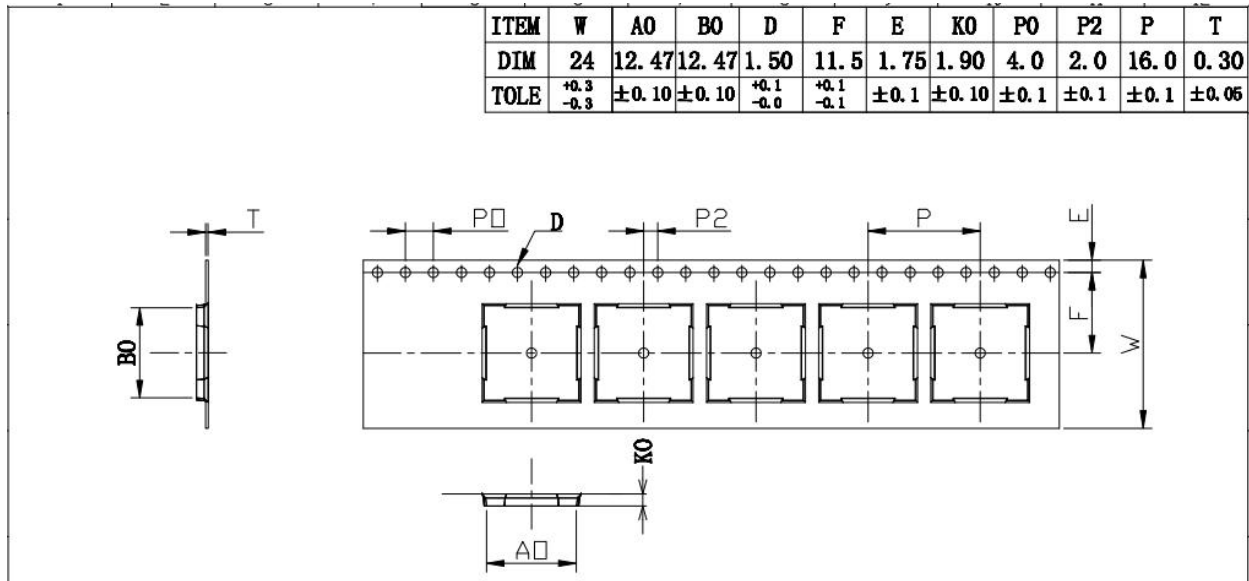
- Calculated shelf life in sealed bag: 12 months at <40°C and <90% RH
- Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5
- The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) is respected
- Baking is required if conditions b) or c) are not respected
- Baking is required if the humidity indicator inside the bag indicates 10% RH or more

## 11 Package

### 11.1 Reel

A roll of 2000pcs





## 11.2 Packaging Detail

the take-up package



Using self-adhesive tape

Size of black tape: 24mm\*32.6m the cover tape : 21.3mm\*32.6m

Color of plastic disc: blue

A roll of 2000pcs



NY bag size:420mm\*450mm



size : 335\*335\*55mm



The packing case size:335\*255\*360mm